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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,790	08/15/2003	Yih-Min Tu	JCLA10858	4787

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EXAMINER	
DSOUZA, JOSEPH FRANCIS A	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,790	TU ET AL.	
	Examiner	Art Unit	
	Adolf DSouza	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Applicant has stated in the Description of the Drawings that Figure 1 is a conventional FSK modulator. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

- On page 6, lines 15 and 22, the word "schematically" should be changed to "showing" to improve the clarity of the description of the drawings.
- On page 9, line 18, "decoder 45" should be changed to "decoder 46" since that is what is shown in Figure 4.
- On page 10, line 1, "with ate least" should be changed to "with atleast".

Appropriate correction is required.

Claim Objections

3. Claim 3 is objected to because of the following informalities: The preamble of the claim should be changed to "A frequency shift keying (FSK) system for.... comprising:" to show the purpose/utility of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 – 2, 4 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suto (US 20030052744) in view of Lansford et al. (US 6,163,568) and further in view of Joshi et al. (US 5,650,754).

Regarding claim 1, Suto discloses a voltage controlled oscillator (VCO) device (page 1, paragraphs 5 – 6), the VCO device comprising:

a switching varactor unit, having a first terminal and a second terminal, wherein the switching varactor unit produces a capacitance, according to a frequency-selection voltage (Fig. 5, elements 121, 511, 512; page 3, paragraph 40; page 4, paragraph 42,

1st 5 lines; wherein the switching varactor unit are the elements 121, 511 and 512, the first and second terminals are the terminals connected to 124a and 124b and the frequency selection voltage is the control voltages outputted from PLL circuit 110);

a VCO core, having a first output terminal, wherein the switching varactor unit is coupled in parallel with the VCO core at the first output terminal and the second output terminal to produce a capacitance effect with respect to the capacitance, so as to adjust a frequency constant of the VCO core (Fig. 5, elements 123 124; page 3, paragraph 40 – 42; wherein the VCO core is interpreted as the combination of the resonance circuit 123 and the high frequency oscillator 124, the output terminal is the terminal 124c and the input terminal is from the output of the PLL circuit 110).

Suto does not disclose that the VCO is used in an FSK system and that the VCO has two output terminals.

In the same field of endeavor, however, Lansford discloses a VCO suitable for use in a frequency shift keying (FSK) system (Fig. 2, element 7c; column 1, lines 6 – 15; column 2, lines 23 – 32).

Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the method, as taught by Lansford, in the system of Suto because this would allow the VCO to be used to generate an FSK signal, as disclosed by Lansford.

In the same field of endeavor, however, Joshi discloses VCO core, having a first output terminal, a second output terminal complementary to the first output terminal, and an input terminal (Fig. 2A, elements 100a, 144a, 146a, 140a; column 6, lines 30 – 35; wherein the two terminals are the 144a and 146a).

Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the method, as taught by Joshi, in the system of Suto because the buffer circuit would provided two isolated outputs, as is well known in the art.

Regarding claim 2, Suto discloses the switching varactor unit comprises a switching diode unit for receiving a mode selection signal with at least one bit data (Fig. 5, element 500c 500b; page 3, paragraph 39 - 40), wherein the switching diode unit includes a plurality of diode pairs coupled in parallel (Fig. 5, elements 121, 511, 512), wherein the diode pairs can be switched on with respect to a quantity of the mode selection signal, so as to produce the capacitance (page 3, paragraph 39; page 4, paragraph 42), wherein the diode pair has one common terminal coupled to the frequency-selection voltage and another terminals coupled to the first terminal and the second terminal, respectively. (Fig. 5, output of PLL circuit 110 fed to element 121 and anodes of the diodes connected to 124a and 124b; page 4, paragraph 42, 1st 5 lines; page 2, paragraph 27).

Claim 4 is similarly analyzed as claim 2.

Regarding claim 5, Suto discloses the diode pairs comprise bipolar junction varactor diode or metal-oxide semiconductor (MOS) varactor diode (page 3, paragraph 33; wherein the bipolar junction varactor diode is interpreted as the PN junction varactor diode).

Claim 6 is similarly analyzed as in claim 2.

Regarding claim 7, Suto discloses the switching varactor unit further comprises a decoder to decode the mode selection signal into a plurality of channels with respect to the diode pairs for use in control the switching device (Fig. 5, element 500; page 3, paragraphs 38 – 39).

6. Claims 3, 8 are is rejected under 35 U.S.C. 103(a) as being unpatentable over Suto (US 20030052744) in view of Lansford et al. (US 6,163,568) and further in view of Joshi et al. (US 5,650,754) and Bomba (US 3,962,640).

Regarding claim 3, Suto discloses:

a switching varactor unit, having a first terminal and a second terminal, wherein the switching varactor unit produces a capacitance, according to a frequency-selection voltage (Fig. 5, elements 121, 511, 512; page 3, paragraph 40; page 4, paragraph 42, 1st 5 lines; wherein the switching varactor unit are the elements 121, 511 and 512, the

first and second terminals are the terminals connected to 124a and 124b and the frequency selection voltage is the control voltages outputted from PLL circuit 110);

and a VCO core, having a first output terminal, a second output terminal complementary to the first output terminal, and an input terminal, wherein the switching varactor unit is coupled in parallel with the VCO core at the first output terminal and the second output terminal to produce a capacitance effect with respect to the capacitance, so as to adjust a frequency constant of the VCO core (Fig. 5, elements 123 124; page 3, paragraph 40 – 42; wherein the VCO core is interpreted as the combination of the resonance circuit 123 and the high frequency oscillator 124, the output terminal is the terminal 124c and the input terminal is from the output of the PLL circuit 110).

Suto does not disclose an FSK system, a frequency selection unit, VCO buffers and a PLL unit coupled to the buffer.

In the same field of endeavor, however, Lansford discloses a VCO suitable for use in a frequency shift keying (FSK) system (Fig. 2, element 7c; column 1, lines 6 – 15; column 2, lines 23 – 32).

Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the method, as taught by Lansford, in the system of Suto because this would allow the VCO to be used to generate an FSK signal, as disclosed by Lansford.

In the same field of endeavor, however, Bomba discloses a frequency selection unit, for receiving an input signal and a mode selection signal, and exporting a frequency-selection voltage according to the mode selection signal (Fig.1, elements 31, 39, 34; column 6, lines 41 – 43; column 8, lines 62 – 64; wherein the frequency selection unit is interpreted as the combination of the elements 31 and 39, the input signal comes from the pulse generator 34, the mode selection signal is signal 41 and the frequency selection voltage that is generated is the output 31t of the ramp generator 31).

Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bomba, in the system of Suto because this would allow the VCO frequency to be changed according to a voltage, as disclosed by Bomba.

In the same field of endeavor, however, Joshi discloses a first VCO buffer, coupled to the first output terminal of the VCO core and exporting a desired frequency and a second VCO buffer, coupled to the second output terminal of the VCO core (column 2, lines 55 – 66; Fig. 1, element 140;wherein the VCO buffer is the element 140. Joshi shows one buffer, which can be used at both outputs of VCO core in the Applicant's invention);

and a phase locked loop unit, coupled between an output of the second VCO buffer and the input terminal of the VCO core to form a feedback loop and produce the desired

frequency (Fig. 1, loop formed by elements 140, 50, 20, 30, ... 100; column 4, line 26 – column 6, line 41; wherein the second VCO buffer is element 140).

Therefore it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the VCO buffers and PLL, as taught by Joshi, in the system of Suto because this would allow isolate the two outputs in a PLL system, as disclosed by Joshi.

Claim 8 is directed to method/steps of the same subject matter claimed in apparatus claim 3 and therefore, is rejected as explained in the rejection of claim 3 above.

Regarding claim 9, Suto discloses the mode selection signal in the switching varactor unit is decoded and turns on corresponding varactor channels of the switching varactor unit, so as to change the capacitance (Fig. 5, element 500; page 3, paragraphs 38 – 42).

Other Prior Art Cited

The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to VCOs whose frequencies are controlled by varactor circuits:

Wynn (US 4,602,222) discloses a circuit for band switching a voltage controlled oscillator.

Martin (US 4,914,695) discloses a Method and apparatus for frequency control of multiple oscillators using a single frequency-locked-loop.

Martin et al. (US 5,686,864) discloses a Method and apparatus for controlling a voltage-controlled oscillator tuning range in a frequency synthesizer.

Bult et al. (US 20010041548) discloses a variable gain amplifier for low voltage applications.

Duncan et al. (US 6,426,680) discloses a system and method for narrow band PLL tuning.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf DSouza whose telephone number is 571-272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
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AD

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SUPERVISORY PATENT EXAMINER